

## **Silicon-on-insulator-based complementary metal oxide semiconductor integrated optoelectronic platform for biomedical applications**

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# Silicon-on-insulator-based complementary metal oxide semiconductor integrated optoelectronic platform for biomedical applications

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**Abstract.** Microscale optical devices enabled by wireless power harvesting and telemetry facilitate manipulation and testing of localized biological environments (e.g., neural recording and stimulation, targeted delivery to cancer cells). Design of integrated microsystems utilizing optical power harvesting and telemetry will enable complex *in vivo* applications like actuating a single nerve, without the difficult requirement of extreme optical focusing or use of nanoparticles. Silicon-on-insulator (SOI)-based platforms provide a very powerful architecture for such miniaturized platforms as these can be used to fabricate both optoelectronic and microelectronic devices on the same substrate. Near-infrared biomedical optics can be effectively utilized for optical power harvesting to generate optimal results compared with other methods (e.g., RF and acoustic) at submillimeter size scales intended for such designs. We present design and integration techniques of optical power harvesting structures with complementary metal oxide semiconductor platforms using SOI technologies along with monolithically integrated electronics. Such platforms can become the basis of optoelectronic biomedical systems including implants and lab-on-chip systems. © 2016 Society of Photo-Optical Instrumentation Engineers (SPIE) [DOI: [10.1117/1.JBO.21.12.127004](https://doi.org/10.1117/1.JBO.21.12.127004)]

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## 1 Introduction

Wireless power harvesting using microscale devices is essential for many smart systems intended for long-term wireless operation in an autonomous mode,<sup>1</sup> including wireless implants embedded within biological tissue. Design of integrated high-efficiency energy harvesting systems will enable use of smart sensors for biomedical applications. In this regard, silicon-on-insulator (SOI)-based photovoltaic devices provide a very powerful design tool as these can be integrated with both optoelectronic and microelectronic platforms. The complementary metal oxide semiconductor (CMOS) integrated SOI platform can be used to implement both electronics as well as optical components. The size scale required for targeted, local biomedical applications, and optical tissue properties (transmission, scattering, and so on) necessitate the use of a suitable wavelength for such applications. Furthermore, CMOS technology provides a powerful platform for signal processing and control operations for such smart implants. Additionally, optoelectronic wireless power harvesting methods can be used efficiently when such devices are located inside a biological environment.<sup>2</sup> Furthermore, such devices can also be integrated with powerful optoelectronic platforms (e.g., the Luxtera platform<sup>3</sup>) to provide high-speed processing capability intended for biomedical systems requiring high-speed operations, e.g., neural probe implants processing significantly large numbers of neurons simultaneously. Combining the principles of biomedical optics with device design will enable efficient power transfer and

telemetry for devices embedded within biological media. Such designs will empower engineers to realize miniaturized system-on-chip devices with integrated photonics, electronics, and wireless powering for completely autonomous operation. There can be many applications of such systems including spectroscopic biosensing,<sup>4</sup> local neural stimulation, and targeted drug delivery.

Reliable powering is an important requirement of practical implants. Conventionally, implants have been powered with transcutaneous wires (e.g., commercial continuous glucose monitoring systems). However, wires pose a permanent risk of infection, irritation, and mechanical damage. Hence, batteries have been used as an alternative power source. However, batteries are bulky and risky since they can leak inside the body and eventually wear out. Hence, a completely autonomous system is ideally powered via wireless sources.<sup>5</sup> Methods to harvest power from ambient power sources (e.g., energy from body's motion, background RF power, thermal energy from body, and so on.) have been explored<sup>6–8</sup> but have very limited energy density for many implant applications.<sup>9</sup> Moreover, these systems need special materials and are difficult to integrate CMOS technology presently. More concentrated wireless powering can be achieved using mechanical waves (acoustic) or electromagnetic waves (RF and optical) generated by a source near the skin surface close to the implant. Efficient generation of acoustic waves requires physically moving devices, e.g., piezoelectric transducers.<sup>10</sup> However, the required materials are not available in standard CMOS process and are inefficient in biological media at short distances, e.g., for subcutaneous implants.<sup>11</sup>

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Hence, acoustic waves have not been used for such power transfer although exciting developments are currently being made in this regard.

Electromagnetic waves do not require a physically moving source and receiver, the size of the devices can be quite small at sufficiently high frequency, and both power density and efficiency can be high for short distances (comparable to wavelength). These methods have been used in the past for many implant applications. For example, near-field inductive coupling<sup>12</sup> and resonantly coupled coils (e.g., Inductive-Capacitive (LC) resonators) have also been tried since Tesla first proposed their use in 1902.<sup>13</sup> Some devices using near-field communication protocols (e.g., radio frequency identification) also use this method for wireless communication over short distances.<sup>14</sup> Far-field electromagnetic powering has also been used for longer distance operations.<sup>15</sup> However, this approach requires a large receiver to harvest sufficient power because of the high path loss in tissue at high frequencies and low energy density of electromagnetic fields in the far-field region.<sup>16</sup> Furthermore, electromagnetic compatibility makes it difficult to use these devices in some environments [e.g., magnetic resonance imaging (MRI) compatibility for biomedical sensors].

Furthermore, due to the ultrahigh frequency (THz range) of optical signals, Photovoltaic (PV) devices can be much smaller in size and can benefit from more focused optical beams to power small devices. PV devices are also MRI compatible and can be used deeper inside the tissue if proper focusing techniques are employed. It has been shown that PV power harvesting can be used with standard CMOS technology to design an integrated system using optical power harvesting, telemetry as well as circuit design on the same platform.<sup>17</sup> However, the output voltage is limited due to bulk CMOS architecture and the design space of electronics circuitry is limited due to the inherent coupling between all devices on the same substrate. Although some special techniques can be used to increase voltage generation by stacking more diodes using special architectures,<sup>18</sup> these are limited to three diodes in series due to the nature of bulk CMOS architecture. Furthermore, bulk CMOS is not an ideal technology if other optoelectronic components (e.g., optical resonators) are to be realized on the same platform.<sup>19</sup>

In this paper, we present design and implementation details of optoelectronic platforms intended for a broad range of biomedical applications and covering a broad range of generation voltage. This integrated design eliminates the requirement of bonding separate photonic and electronic components, greatly simplifying system implementation. As an example, we use CMOS technology to realize SOI-based PV devices along with standard electronics circuitry on the same substrate resulting in a completely integrated and planar system. The same design and implementation principles can be used for many other subsystems, e.g., metabolic sensors.

In the Secs. 2, 3, and 4, we present system design and implementation techniques, provide details of device processing in Sec. 5 and compare our results with the wireless power harvesting using other techniques in Sec. 6.

## 2 Technology Selection

Silicon is the standard material used for fabrication of micro-electronic and optoelectronic systems. Standard or bulk CMOS technologies use the same silicon substrate for all the devices on a die. This results in a fundamental limitation in

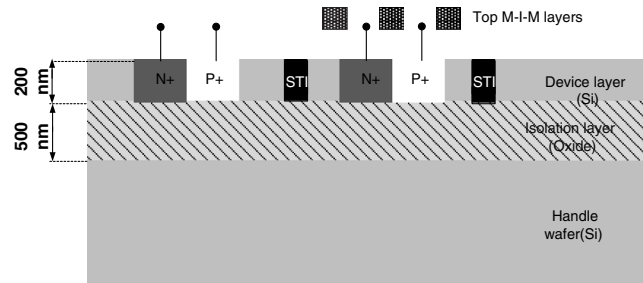


Fig. 1 Architecture of SOI-based CMOS technology.

creating isolation between different devices.<sup>20</sup> For power harvesting systems, this means stacking up more PV devices in series to achieve higher voltages is challenging. Furthermore, power supply noise also becomes an issue for autonomous system operation, especially if switching is required (e.g., for oscillators, digital circuitry).

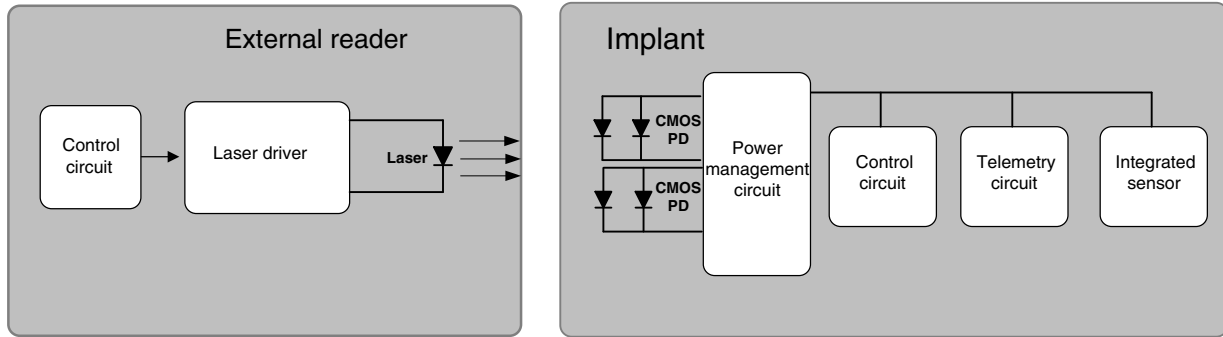
Use of SOI devices can be effective in generating higher voltages and isolating electronic and optical components due to inherent device isolation. However, the photogeneration region is substantially thinner in SOI-based CMOS technologies (Fig. 1) than in bulk CMOS, severely limiting the PV output current.<sup>21</sup> For applications in which both high voltage and high current is required (e.g., neural stimulation, optical telemetry from biomedical implants using microlasers, and so on), special techniques are required to optimize the SOI-based PV devices for such applications.

Wavelength of operation is also an important design consideration as absorption depth of light in a material is wavelength dependent. Silicon devices should have thickness on the order of absorption depth to be able to efficiently absorb the incident light.<sup>21</sup> Moreover, absorption and scattering in the medium between the wireless system and optical power source is also important. For optical powering of wireless implants, absorption in the skin and tissue needs to be minimized while maximizing absorption in the PV devices. The near-infrared (NIR) region is very suitable for implantable applications due to the presence of a region of low losses in the tissue that overlaps with suitable wavelengths which can be absorbed in silicon photovoltaic devices. This so called “therapeutic window” is quite suitable for transmission of photons through the skin and the tissue.<sup>22</sup> Although this wavelength region is not optimal for the relatively thin (e.g., 200 nm) silicon region available in commercial CMOS-based SOI devices (Si absorption depth in NIR is near  $10\ \mu\text{m}$ <sup>23</sup>), it is the most suitable choice for our applications due to the system level constraints on high optical power transmission through the biological tissue. The limitation in device thickness compared to absorption depth will be addressed by optimized device design as presented in Secs. 4 and 5.

## 3 System Design

The presented system consists of an integrated implant having SOI-based PV devices, a power management circuit and rest of the circuit based upon system applications (e.g., a control circuit, a telemetry circuit, and an integrated sensor). An external reader device is used to power the implantable device (Fig. 2).

The electronics is covered with unused top metal layer(s) to minimize the effect of high intensity optical illumination used for wireless powering. The optoelectronic part consists of integrated PV devices, integrated photodiode structures used as



**Fig. 2** Schematic representation of integrated optoelectronic system design.

sensors (photodetectors) and compound semiconductor-based laser for telemetry. Optical component design relies on silicon-buried oxide-silicon-based structure under multilayer dielectric and metal structure [aka metal–insulator–metal (MIM) structure] of the SOI-CMOS process. This SOI structure can be used to realize silicon resonator structures for dense optical multiplexing<sup>24</sup> that can be used in biomedical applications, e.g., for multiplexing large-scale neural data.

For SOI technologies, only lateral p–n junctions are used as PV devices since vertical junctions are not available due to thin device layer. The absorption depth of light in silicon in the NIR wavelength range is on the order of few microns<sup>23</sup> whereas substrate thickness is only few hundreds of nanometers. Hence, design optimization techniques are required to increase the photogenerated current. One important optimization technique is using the top metal layers as optical reflectors using backside illumination since the top side is covered with MIM structure in most areas. Another technique is using focused energy beams, i.e., lasers to increase photovoltaic output. Optical focusing within the tissue also increases system efficiency by focusing more light on the implanted device.

The photogenerated current from a p–n junction photovoltaic device is the current due to electron–hole pair generation due to photon absorption. For most cells with small series resistance, short circuit current and photogenerated current are almost equal. Hence, the short circuit current is equal to photocurrent density given by<sup>21</sup>

$$J_{sc} = q(L_n + L_p + W_d)G, \quad (1)$$

where  $q$  is the electronic charge and  $G$  is the photogeneration rate. Since the useful photogeneration region is the depletion region ( $W_d$ ) and minority carrier diffusion regions ( $L_n, L_p$ ), the PV devices are designed as distributed photodiode structures to minimize bulk regions which do not contribute significantly to generated current. For our design, the device structure was designed using the design rules of the actual SOI-CMOS process. shallow trench isolation was used between the distributed photodiode architecture to ensure proper isolation, as shown in Fig. 3.

The optical generation rate ( $G$ ) at depth  $x$  depends upon incident optical intensity ( $I_o$ ), device cross-section area ( $A$ ), depth ( $x$ ), and the absorption coefficient ( $\alpha$ ) which represents conversion of optical intensity into electron–hole pairs, according to the following equation:<sup>21</sup>

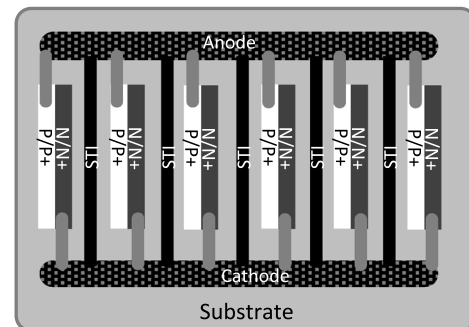
$$G(x) = \frac{\alpha I_o}{A} e^{-\alpha x}. \quad (2)$$

Hence, the total current in a lateral SOI-PV device is the integration of the current across the lateral cross-section of the device. The open circuit voltage of a single PV device is given by the following equation:<sup>21</sup>

$$V_{OC} = \frac{nkT}{q} \ln\left(\frac{J_{sc}}{J_o} + 1\right), \quad (3)$$

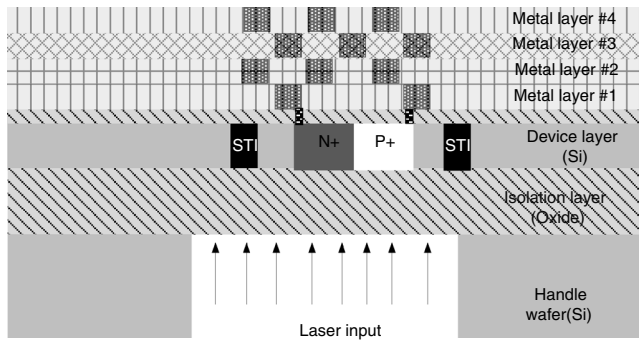
where  $n$  is the quality factor of the junction,  $T$  is the absolute temperature of the junction,  $q$  is the electronic charge,  $k$  is the Boltzmann Constant,  $J_{sc}$  is the short circuit current density, and  $J_o$  is the reverse saturation current density. This shows that high illumination intensity and good junction quality are required to generate high device voltage.

Within a PV module, metal contact lines are used to connect the distributed photodiode structures. If front illumination is used, these metal structures decrease system efficiency by reflecting a significant portion of incoming light. However, if backside illumination is used, this design allows us to use the front multilayer metal structure to reflect the optical signal back to thin silicon absorption area. Due to CMOS design rules, the metal structure needs to be designed as a grid and optimization of this grid structure can help enhance this effect. When backside illumination is used, the backside silicon handle wafer has to be removed to allow light to reach the active (device) layer. The transmission of buried oxide (BOX) in the near-infrared region is more than 80%;<sup>21</sup> hence, it is not removed in our design to increase the mechanical integrity of the thin membrane after etching. Due to the thin nature of silicon and the BOX layer, the heat capacity of thin membrane is low. Silicon is an indirect bandgap material and hence its temperature can increase during optical illumination. However, the BOX layer does not heat up significantly during optical illumination and hence can provide conductive cooling to the active device layer



**Fig. 3** Design of SOI-CMOS PV cell.





**Fig. 4** Schematic representation of system design for backside illumination.

along with the top interlayer dielectric structure. Furthermore, stacked metal layers can be used to scatter incoming light to increase the optical path length within the silicon absorption area. The complete device design is shown in Fig. 4.

Another technique to increase the photocurrent is to design a mirror structure using frontal metal layers and backside BOX layer. However, due to the high transmission through the BOX layer, the mirror structure between front metal structures and the BOX layer will not be very efficient. Furthermore, lack of control on structural elements in the CMOS fabrication process makes it challenging to control system design to enhance this mirror effect. However, further CMOS postprocessing can be used to enhance this effect and increase the local light intensity to increase overall signal absorption, similar to the design of vertical cavity surface emitting lasers.

#### 4 System Implementation

The SOI-CMOS-based PV devices were designed and fabricated using the ST 130 nm HCMOS9SOI process offered through the CMP service. Electrical circuit design consists of a basic signal processing circuit using a ring resonator and a simple tuned LC coil as a test receiver. Optoelectronic design consists of a PV-based power harvesting system using four photodiodes connected in series by lower layer metal connections (Fig. 5). The layout depicts the trench isolation structures that are used to ensure isolation between the four photodiodes.

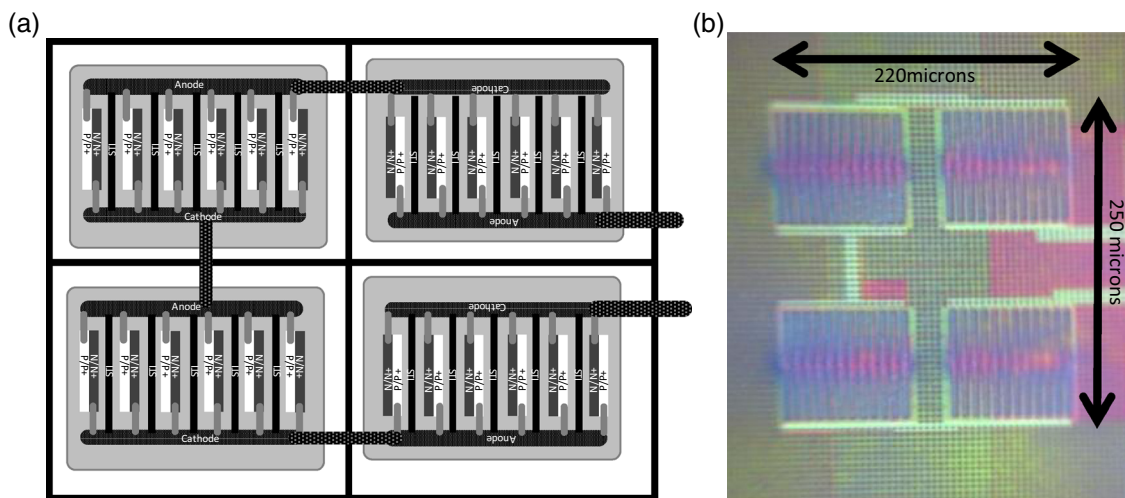
Top layer metals were used to form a metal grid to reflect the optical signal back to the silicon absorption area to maximize absorption in the device layer. The metal grid design was dictated by the CMOS design rules. A multilayer metal grid structure was designed to create multiple reflections from the metal stack back to the device active area. Devices with different designs and device connections were fabricated to test system performance as the devices are scaled to smaller and smaller dimensions.

#### 5 Device Processing

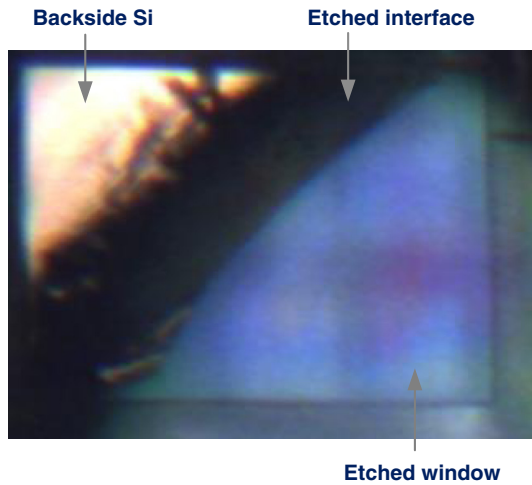
In the SOI-CMOS process, the PV devices are fabricated on the thin top silicon layer (i.e., the device layer). Most of the area of these devices is covered with metal contact pads and other top metal layers used for routing and filling requirements of the CMOS process. For backside illumination, the SOI handle wafer is removed to allow optical access to the PV structures, as shown in Fig. 6.

For our applications, the handle substrate ( $\sim 750\text{-}\mu\text{m}$  thick) was first thinned down (to around  $100\text{-}\mu\text{m}$  thickness) and then etched selectively. The thinning process was done using a lapping machine employing a SiC sand paper. Alternatively, anisotropic etching using xenon difluoride was used for this purpose. After thinning down, etching windows were opened underneath the PV devices using backside aligned lithography in a Carl Suss MA6 aligner. AZ5214E resist was used as etch mask. Postbaking was used to get rid of any moisture which negatively affects the xenon difluoride ( $\text{XeF}_2$ ) etch. This was followed by pulsed  $\text{XeF}_2$  etching to remove the handle wafer to expose the devices for backside illumination. For photonics structures using standard CMOS-based SOI processes, the bulk silicon wafer can be etched to a controlled depth to precisely control the properties of the photonics device.

After etching, the frontal structures are visible from the back side via optical microscopy. scanning electron microscope images of the device show complete removal of the back silicon substrate. The etch window can be filled with suitable polymer material, providing index matching to serve as an antireflective coating as well as to improve thermal dissipation. The front metal structures were designed according to the design rules of the SOI-CMOS process. Both contact lines and CMOS fill layers were used to create efficient reflection of light back to



**Fig. 5** PV system showing series connection of four photodiodes (a) layout and (b) actual die.



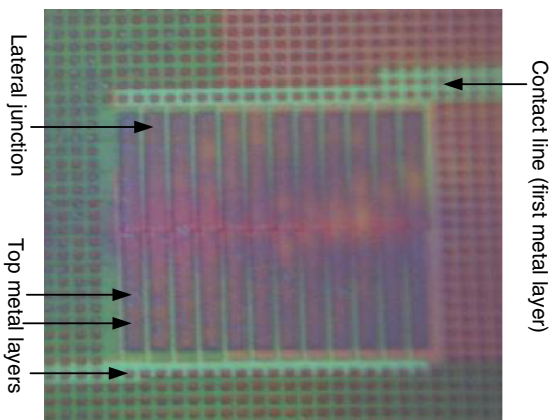
**Fig. 6** Backside etching to remove Si handle wafer.

the device layer, when backside illumination is used, as shown in Fig. 7.

Pulsing the incident laser is a useful technique to increase the instantaneous output power. This allows using higher laser intensities for short periods to achieve larger current pulses. For many applications, this is acceptable as the pulsing duration and rate can be programmed according to the requirements. For example, in sensing applications, the sensor can be powered periodically to measure its response and the period can be designed according to the application. The highest allowable pulsing rate depends upon the thermal properties of the surrounding tissue and CMOS structures.

## 6 Testing and Results

The fabricated devices were tested electrically and optically to quantify their performance. The dies were mounted on a chip carrier and the device pads were wire bonded to PCB pads (Au) for testing. For backside illumination, the devices were first processed in a clean room environment and were then mounted on a glass slide with gold thin film (200-nm Au on 200-nm Ti) contact traces. The device contact pads were wire bonded with the contact lines on the glass slide. The contact pads on the glass slide were used to make electrical contacts with electrical probes while the chip was illuminated from the back side through glass slide.



**Fig. 7** Backside view showing device and metal layers.

## 6.1 Testing

A semiconductor parameter analyzer (HP 4155) and an electrical probe station (Cascade Microtech) were used to perform electrical testing of the devices. The setup used to optically test these devices consisted of a high power NIR laser (0.8 W, 805 nm), a Keithley Source Meter (2400) and an optical table setup for alignment. The laser was used in pulsed mode utilizing a mechanical shutter from Thorlabs. The maximum operation frequency of the shutter was 40 Hz. Power laser focus was adjusted to control the laser spot size and consequently the optical input intensity for the PV devices. The PV devices were characterized for free space operation as well as for operation through biological tissue (chicken skin and tissue).

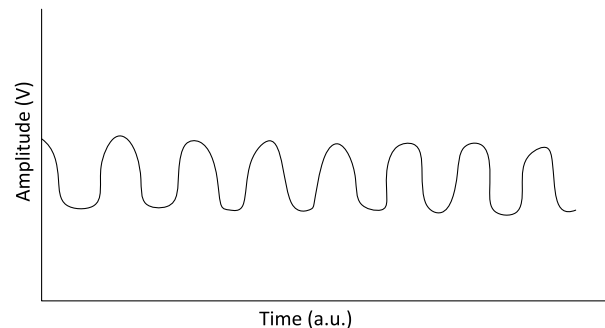
## 6.2 Results

The electronics circuits consisting of ring resonators performed as designed (Fig. 8) without being affected by rest of the optoelectronic circuitry. This shows complete isolation between the system components allowing for much simpler and robust design of complicated systems.

Electrical testing of PV devices also confirmed that proper isolation was achieved between the electronic and optical components of the system. It further revealed isolation between the individual photodiodes within the PV modules as required from the SOI process. Since these were custom designed devices, these isolation structures were designed to ensure isolation between different subsystems as well as between photodiodes within the PV modules to create high series voltage. Stacking of multiple PV modules allowed us to achieve as high as 12 V without any isolation issue. Optoelectronic testing confirmed that this isolation was not affected during optical illumination of the devices, which is contrary to standard CMOS in which optical illumination of PV devices create leaky paths owing to stray devices formed in the bulk substrate.<sup>20</sup>

Different geometric variants of PV modules were designed and fabricated to provide insights into the benefits of the custom distributed design topology. It was expected that the design with the highest lateral junction area will provide maximum output power compared to the other devices. Two different designs are shown in Fig. 9 for comparison. The gray area denotes the n-doped well and the white area denotes p/p+ doped areas.

The results (Table 1) confirmed that the distributed design provided much better performance (high short circuit current) compared to the standard cell design based upon one p-n junction. Subsequently, this optimized design was used for all further testing. It was confirmed that overall output power was



**Fig. 8** Output of CMOS integrated oscillator circuit.

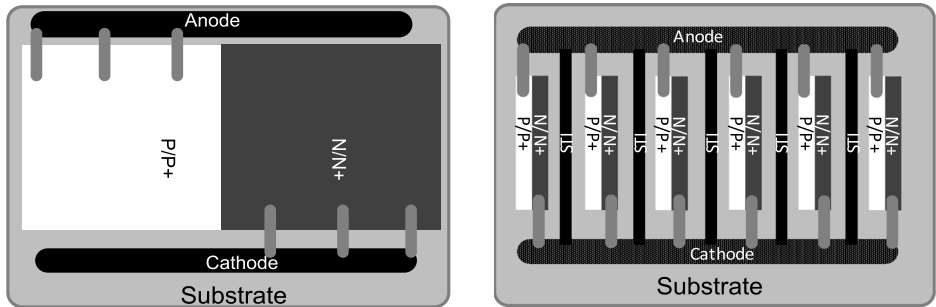


Fig. 9 Photodiode geometries for the SOI-CMOS PV design comparison.

Table 1 Photodiode geometry comparison.

Design	Open circuit voltage (V)	Short circuit current ( $\mu\text{A}$ )
Single diode	0.7	20
Distributed diode	0.65	50

proportional to the area of the device. This is also in contrast to the bulk CMOS technology in which substrate leakage limits the device performance and it is quite challenging to increase the output of the PV module by simply increasing the device area.<sup>20</sup>

Devices were tested under both topside illumination and backside illumination mode and the results were compared, as shown in Fig. 10, confirming the advantage of backside illumination scheme. For backside illumination, maximum input power was limited by the thermal properties of the membrane structure after the handle wafer was etched.

Pulsed mode allowed us to use a higher input power for shorter duration to increase optical signal output for a short time period. The safe operation of continuous and pulsed mode (laser output power and illumination duration that maximizes output signal without mechanically damaging the device layer) was also compared, as shown in Fig. 11. The pulsing parameters are also dependent upon surrounding media (due to conductive and convective cooling in the body) and hence a longer pulsing is possible for operation of tissue embedded sensors compared with one in air.

The laser illumination power was controlled by controlling the laser spot size on the device by adjusting its focus. The laser output power was fixed to 0.8 W at 805 nm. The spot size was adjusted to control the intensity of the laser spot on the device. The pulsed mode resulted in higher output power as the input power was higher, without damaging the PV system in both cases (laser spot size was adjusted to be  $\sim 20 \text{ mm}^2$  for pulsed mode,  $80 \text{ mm}^2$  for continuous mode). At the given switching speed of the shutter (40 ms on-time every minute), the turn-on and turn-off delays of the PV system were negligible. From these results, the best case efficiency can be calculated to be around 10% for both continuous and pulsed mode. This is similar to that reported by other researchers working on PV devices illuminated by monochromatic illumination.<sup>25</sup>

The expected output of the design without the metal grid is calculated by determining the percentage of absorbed input optical signal and assuming that all of it is converted into electrical current at the device terminals. Using Eq. (1), for 805-nm (photon energy of 1.5 eV) laser with 0.8-W power at  $20\text{-mm}^2$  spot size, using typical doping densities of  $5 \times 10^{17}$  for P region and  $10^{18}$  for N region, the best case current (assuming 100% quantum efficiency) generated for  $100 \mu\text{m} \times 100 \mu\text{m}$  device with 200-nm thick silicon layer with an optical intensity  $I = \frac{0.8 \text{ W}}{20 \text{ mm}^2}$  is on the order 22 pA as per the following relationships

$$G = \frac{I}{E_{\text{Photon}}}, \quad (4)$$

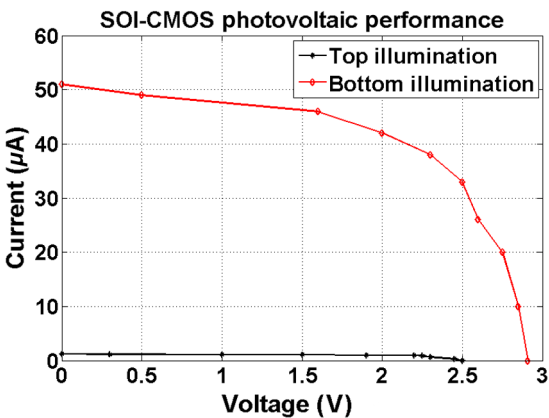


Fig. 10 Comparison of device performance for top versus bottom illumination.

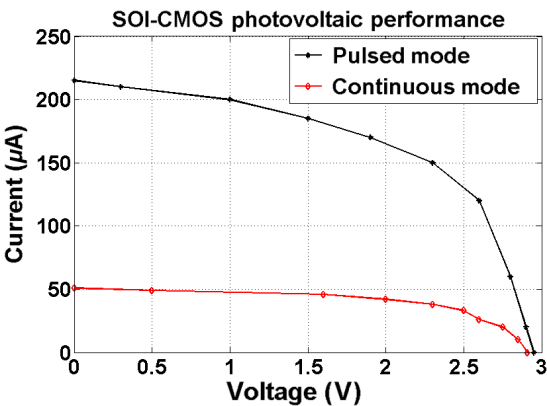


Fig. 11 Comparison of continuous versus pulsed backside illumination.



$$I_{PV} = qA(L_n + L_p + W_d)G. \quad (5)$$

The measured current with optical reflection is orders of magnitude more (e.g., 215 nA), indicating the current enhancement due to multiple reflections and due to some local optical trapping effects increasing the optical absorption in the device.

Furthermore, for thermal calculations, the absorbed energy in silicon is found using the exponential absorption model. Each absorbed photon has energy ( $E_{ph}$ ) higher than silicon bandgap ( $E_{si}$ ) and this difference is absorbed in the silicon slab as thermal energy ( $E_{th}$ ). For a given number of photons absorbed over a certain time interval, the total energy delivered to the silicon slab and the resulting temperature increase can be calculated from this resulting heat source according to the following equations:

$$Q_{abs} = E_{th}N_{ph}, \quad (6)$$

$$T_{Si} = \frac{Q_{abs}}{m_{Si}C_{Si}}. \quad (7)$$

In practice, the energy absorbed by the silicon layer is higher due to multiple reflections as indicated by higher device current as discussed previously. Hence, the actual temperature increase is higher than the one predicted by single pass of optical signal through the silicon device layer.

However, the BOX layer and the top CMOS layers help in cooling down the Si layer, as shown by thermal model of Fig. 12. When the input intensity is increased beyond the experimental limits of the test setup (i.e., 20-mm<sup>2</sup> spot size), the device layer would fail thermally indicating that the actual temperature increase is much higher than that predicted by simple single-pass absorption model.

Finally, the effect of biological tissue was measured by inserting a piece of chicken skin (~2-mm thick) between the illumination laser and the device. The results are shown in Fig. 13.

As expected, the PV response decreased substantially due to the tissue. For the case of light passing through biological tissue, light intensity at depth  $x$  inside the tissue is given by

$$I(x) = \Gamma I_o e^{-[\alpha(\lambda) + \mu'_s]x}, \quad (8)$$

here  $\Gamma$  is the reflection coefficient of skin,  $I_o$  is the incident intensity of light,  $\alpha$  is the absorption coefficient, and  $\mu'_s$  is the reduced scattering coefficient. Using typical parameters of 2-mm thick skin at 805-nm wavelength ( $\alpha = 0.1 \text{ mm}^{-1}$ ,  $\mu'_s = 1.2 \text{ mm}^{-1}$ ,  $\Gamma = 0.8$ <sup>26</sup>), we can calculate that the light reaching the CMOS implant will be 1.5% of incident light.

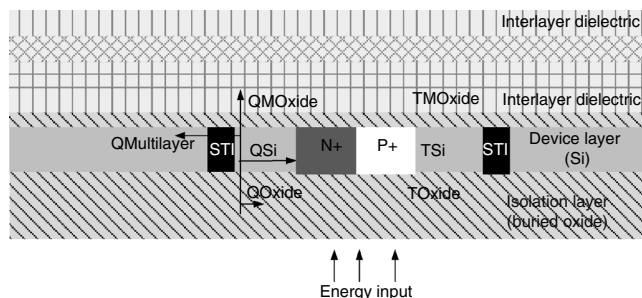


Fig. 12 Simplified device model for thermal analysis.

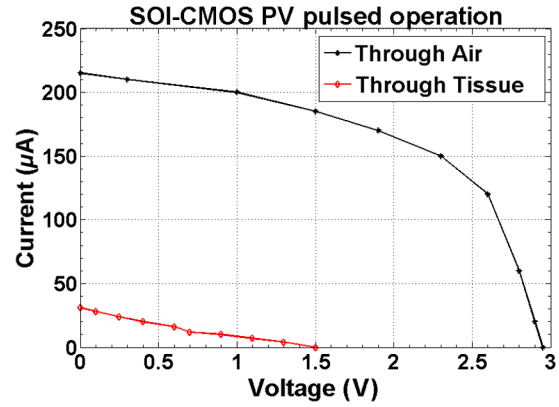


Fig. 13 Comparison of PV response from air and through biological tissue.

This is because of scattering and absorption due to the intricate structure of skin (Fig. 14). The experimental efficiency was calculated as the ratio of incident power (laser intensity multiplied by device area) and photogenerated power (power at maximum power point on the  $V-I$  curve). The efficiency of the system when illuminated without the tissue is around 10% (calculated assuming all incident laser power lies within a narrow band around the 805-nm wavelength). After including the effect of biological tissue, the calculated efficiency decreased from 10% in air to 1.8% in tissue which is quite close to the calculated results. The difference can be attributed to the difference between the theoretical case and the experimental setup (multiple reflections, tissue parameters different from actual model). Further enhancements in efficiency are possible by utilizing techniques to improve laser focus inside the tissue. There are several methods including use of acoustic waves to focus optical signals inside the biological tissue.<sup>27</sup>

Although the signal drop due to tissue is significant, the output power is still quite significant for the small size scale device embedded within the tissue and can be used to power complex CMOS systems utilizing low-power design. When compared with RF and bulk CMOS-based PV devices, the SOI-CMOS devices provide higher efficiency for *in vivo* operation (Table 2) for the near-millimeter size implantable devices. This is mainly due to better performance of optical devices at subwavelength

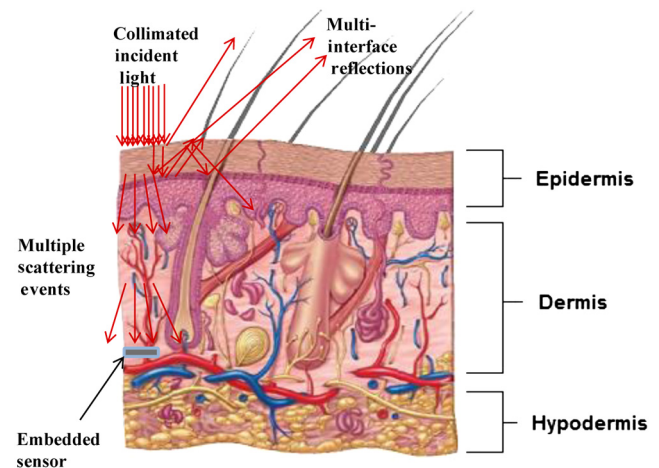


Fig. 14 Effect of biomedical tissue on optical illumination of subdermal implant.



**Table 2** Comparison of SOI-CMOS-based PV devices with RF and bulk CMOS-based PV devices.

Parameter (for operation in biological media)	Near-field RF [bulk CMOS (180 nm)] <sup>14</sup>	Optical [bulk CMOS (250 nm)] <sup>20</sup>	Optical [SOI- CMOS (130 nm)] (this work)
Efficiency (%)	0.2	0.4	1.8
Short-circuit current ( $\mu$ A)	8	25	31
Open-circuit voltage (V)	1.2	1.4	1.5

size scale compared with RF devices. Furthermore, SOI-CMOS devices are far less affected by leakage and parasitic devices compared to bulk CMOS devices. This result in more photogenerated power being available to load and less power wasted due to leakage effects. The above analysis applies to photodiode structures in the SOI process. Since some SOI processes can have lower performance compared with bulk CMOS devices in terms of overall power consumption (high off current), a detailed power balance analysis should be considered before making the final selection of suitable architecture for a particular application.

The power levels used in this work are all within the safety tolerances of NIR illumination used for biological media.<sup>28</sup> Hence, the proposed system can actually be used for practical applications.

## 7 Conclusion

In this work, we presented an optoelectronic SOI-based CMOS system design for wireless biomedical applications. The system utilizes integrated power harvesting devices for implants located within biological tissues (e.g., subcutaneous region) along with monolithically integrated electronics. We demonstrated that both electronic and optical components can be designed using this architecture and excellent isolation between these is achieved by using trench isolation structures. Although a simple ring oscillator circuit was used to demonstrate this, advanced circuits can be designed in principle without any restriction. Furthermore, we also demonstrated that sufficiently high voltages and currents can be generated from miniaturized integrated photovoltaic devices if concentrated monochromatic (e.g., laser) light is used to illuminate the devices from backside, after a suitable illumination window is formed by etching the handle wafer and a multilayer reflection structure is designed in the top metal layers. We also showed that a distributed design allows for a higher photocurrent compared to standard photodiode structure. Such miniaturized implants can achieve much smaller size scale (i.e., in submillimeter range) compared with those possible by magnetic, RF, and acoustic power transfer. Additionally, system level monolithic integration can be used to design extremely powerful systems with a standard commercial and scalable manufacturing process, reducing cost and complexity significantly. The architecture presented in this work should be analyzed for each application in terms of specifications (power consumption, device size, cost, and voltage requirement) before making a final selection.

## Disclosures

Authors report no financial conflict of interest regarding this publication. In addition, authors have a patent silicon-on-insulator based sensor architectures pending.

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